SEMICONDUCTOR CASSETTE REDUCER

Field of the Invention

The present invention relates generally to the field of semiconductor processing tools and more particularly to a semiconductor cassette reducer.

Background of the Invention

Semiconductor wafers are produced in a number of different sizes. Older facilities typically have smaller size wafers. The size of wafers has increased over time as technology has advanced. As the size of the wafer increases the cost of processing each wafer increases. In order to justify larger wafer sizes the defect rate for each wafer must be low enough to provide a satisfactory yield. As a result, semiconductor processing facilities may want to prove out a design using smaller size wafers. This reduces the cost of mistakes. Unfortunately, the latest and best processing equipment is generally designed to processes the largest wafers. The wafers are held in containers called front opening unified pods (FOUPs). A FOUP 10 is shown in FIG. 1. Thus there exists a need

for a device that allows facilities to use the latest processing equipment without being required to process the largest wafers.

Brief Description of the Drawings

FIG. 1 is a perspective view of a front opening unified pod;

FIG. 2 is an exploded view of a semiconductor cassette reducer in accordance with one embodiment of the invention; and

FIG. 3 is a top left view perspective of a semiconductor cassette reducer in accordance with one embodiment of the invention.

Detailed Description of the Drawings

A semiconductor cassette reducer has a first substantially U-shaped plate and a second substantially U-shaped plate. A number of wafer supports connect the first substantially U-shaped plate to the second substantially U-shaped plate. Several retention springs are attached to the first substantially U-shaped plate. The retention springs hold the semiconductor cassette reducer in a FOUP (front opening unified pod).

FIG. 2 is an exploded view of a semiconductor cassette reducer 20 in accordance with one embodiment of the invention. The semiconductor cassette reducer 20 has a first substantially U-shaped plate 22 and a second substantially U-shaped plate 24. A plurality of wafer supports 26, 28, 30, 32 connect the first substantially U-shaped plate 22 to the second substantially U-shaped plate 24. In one embodiment screws 34 and washers 36 are used to attach the U-shaped plates 22, 24 to the wafer supports 26, 28, 30, 32. Retention springs (plurality of retention springs, more than two retention springs, flexible disks) 38 are attached to the first U-shaped plate 22 and the second U-shaped plate 24. In one embodiment, the retention springs 38 are attached using screws 40. In one embodiment, the retention springs are formed of a rubbery substance that is deformable. When the cassette reducer is placed in the FOUP the retention springs 38 grab the sides of the FOUP. The back two retention springs 38' lock into a depression (lip) in the FOUP. This provides a solid grip for the cassette in FOUP. The

retention springs also make it very easy to insert and remove the cassette from the FOUP.

In one embodiment, the U-shaped plates 22, 24 have a pair of interior arm cutouts (first arm cutout) 42. The cutouts 42 allow the end effector of a robot arm easy access to the wafers in the cassette reducer 20. The U-shaped plates 22, 24 also have a base cutout 44. The base cutout also makes it easier for the end effector to access wafers. The U-shaped plates have a pair of arms 45. In one embodiment, a base 46 to tip 48 distance 50 is less than an interior depth 52 (see FIG. 1) of a front opening unified pod. In one embodiment, the U-shaped plates 22, 24 have an exterior partial S-shaped cutout 53. These S-shaped cutouts are necessary for the U-shaped plates to fit inside certain FOUP designs.

The plurality of wafer supports 26, 28, 30, 32 include a pair of side panels (wafer support panel) 30, 32. The side panels have a plurality of lips 54. The lips hold the semiconductor wafers. The plurality of wafer supports 26, 28, 30, 32 also includes a pair of columns (column wafer supports) 26, 28. The columns 26, 28 have a first position 56 and a second position 58. The first position allows the wafers to be coaxially aligned with the position of the larger wafers in the FOUP and the second position aligns the front edge of the wafer with the front edge of the FOUP.

FIG. 3 is a top left view perspective of a semiconductor cassette reducer 20 in accordance with one embodiment of the invention. The cassette reducer 20 fits inside of the FOUP of figure 1. In one embodiment, the FOUP is designed to hold 300mm diameter semiconductor wafers and the cassette reducer 20 holds 200mm

diameter semiconductor wafers. FIG. 3 shows the semiconductor cassette reducer 20 assembled. The same reference numerals are used for both figures.

Thus there has been described a semiconductor cassette reducer that is easy to install and allows semiconductor facilities to use the latest processing equipment without being required to process the largest wafers.

While the invention has been described in conjunction with specific embodiments thereof, it is evident that many alterations, modifications, and variations will be apparent to those skilled in the art in light of the foregoing description. Accordingly, it is intended to embrace all such alterations, modifications, and variations in the appended claims.